

# High Speed Layout Design Guidelines

## MC9328MX1, MC9328MXL, and MC9328MXS

### 1 Abstract

Design of memory systems becomes more complex as the operation frequency increases in a low-power environment. A number of criteria should be considered to achieve maximum system performance under these conditions. The i.MX external memory bus is intended to work with PC100 grade memory. Care must be taken in board layout to achieve a system capable of maximum bus rates at low voltage.

This document describes the recent investigation into the maximum memory bus frequency of a low-power memory system in terms of stability, capacitive loading, and production margin. This data will be useful to customers in their design of low power high speed memory systems with the i.MX applications processors

This document applies to the following i.MX devices, collectively called i.MX throughout:

- MC9328MX1
- MC9328MXL
- MC9328MXS

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## 2 Design Consideration

To achieve high speed operation in a low-power environment, the design of the PCB must achieve:

- Minimal on-board noise generation from the distributed power network
- Minimal cross-talk between traces
- Reduction of ground bounce effect
- Simultaneous switching noise during the operation
- Impedance matching by the proper setting on the I/O pad driving strength against the target memory bus loading
- Provide correct signal line termination

### 2.1 Board Material

Printed Circuit Board (PCB) dielectric construction material controls how much noise and cross-talk is contributed from the fast switching I/O signals. This dielectric material can be assigned a dielectric constant ( $\epsilon_r$ ) that is related to the force (see [Equation 1](#)) of attraction between two opposite charges separated by a distance in a uniform medium.

$$F = (Q_1 Q_2) / (4\pi \epsilon r^2) \quad \text{Eqn. 1}$$

Where  $Q_1$  and  $Q_2$  are charges,  $r$  is distance between the charges (m),  $F$  as force (N) and  $\epsilon$  is permittivity of dielectric (F/m). Each PCB substrate has a different relative dielectric constant. The dielectric constant is permittivity of a relative to that of empty space, see [Equation 2](#).

$$\epsilon_r = \epsilon / \epsilon_0 \quad \text{Eqn. 2}$$

Where  $\epsilon_r$  is dielectric constant,  $\epsilon_0$  is permittivity of empty space (F/m), and  $\epsilon$  is permittivity (F/m). The dielectric constant compares the effect of an insulator on the capacitance of a conductor pair, to the capacitance of the conductor pair in a vacuum. The dielectric constant affects the impedance of a transmission line, and signals can propagate faster in materials that have a lower  $\epsilon_r$ .

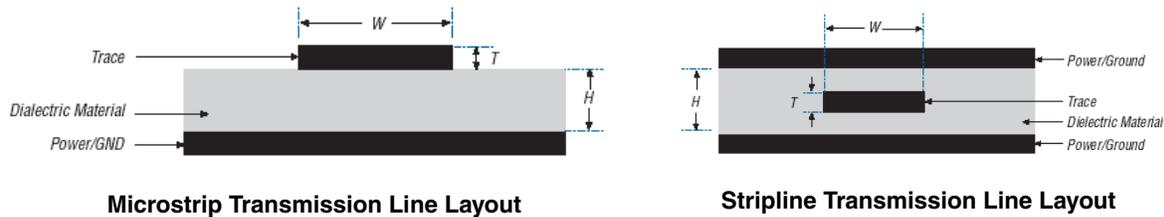
A high-frequency signal that propagates through a long line on the PCB from driver to receiver is severely affected by the loss tangent of the dielectric material. A large loss tangent means higher dielectric absorption. Material with a high loss tangent value affects the high frequency signal on a long line. Dielectric absorption increases attenuation at higher frequencies. [Table 1](#) shows the loss tangent value for FR-4 and GETEK materials.

The most widely used dielectric material for PCBs is FR-4, a glass laminate with epoxy resin that meets a wide variety of processing conditions. The  $\epsilon_r$  for FR-4 is between 4.1 and 4.5. GETEK is another material that can be used in high speed boards. GETEK is composed of epoxy and resin (polyethylene oxide) and has an  $\epsilon_r$  between 3.6 and 4.2.

**Table 1. Loss Tangent Value of FR4 and GETEK Materials**

Manufacturer	Material	Loss Tangent Value
GE Electromaterials	GETEK	0.010 @ 1MHz
Isola Laminate Systems	FR-4	0.019 @ 1MHz

Another factor to affect signal performance and noise separation is transmission line effect and modeling. Transmission line is a trace, and has a distributed mixture of resistance (R), inductance (L), and capacitance (C). There are two types of transmission line layouts: Microstrip and Stripline. Figure 1 shows the two types of transmission line layouts.



W = width of trace, T = thickness of trace, and H = height between trace and reference plane

**Figure 1. Transmission Line Layout**

Any circuit trace on the PCB has characteristic impedance associated with it. This impedance is dependent on width (W) of the trace, thickness (T) of the trace, dielectric constant ( $\epsilon_r$ ) of the material used, and height (H) between the trace and reference plane.

### 2.1.1 Microstrip Impedance

A circuit trace routed on an outside layer of the PCB with a reference plane (i.e., GND or Vcc) below it, constitutes a microstrip layout. Use Equation 3 to calculate the impedance of a microstrip trace layout.

**Eqn. 3**

$$Z_o = \frac{87}{\sqrt{\epsilon_r + 1.41}} \cdot \log\left(\frac{5.98 \times H}{0.8W + T}\right) \cdot \Omega$$

Using the typical values of W = 8 mil, H = 5 mil, T = 1.4 mil,  $\epsilon_r$  and (FR-4) = 4.1 with and solving for microstrip impedance (Z) yields the results shown in Equation 4, Figure 2, Figure 3, and Figure 4. The measurement unit in Equation 3 is mils (i.e., 1 mil = 0.001 inches). The copper (Cu) trace thickness (T) is usually measured in ounces (i.e., 1 oz. = 1.4 mil).

**Eqn. 4**

$$Z_o = \frac{87}{\sqrt{4.1 + 1.41}} \cdot \log\left(\frac{5.98 \times (5)}{0.8(8) + 1.4}\right) \approx 50\Omega$$

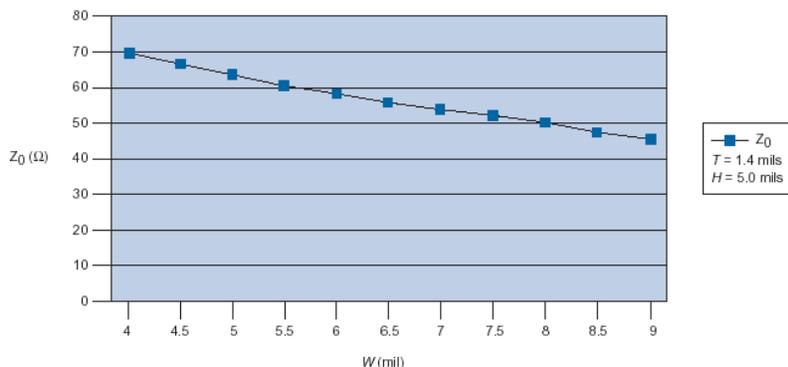


Figure 2. Microstrip Trace Impedance vs. Trace Width (W)

This figure shows the microstrip trace impedance vs. trace width (W) using values in Equation 3, keeping dielectric height and trace thickness constant.

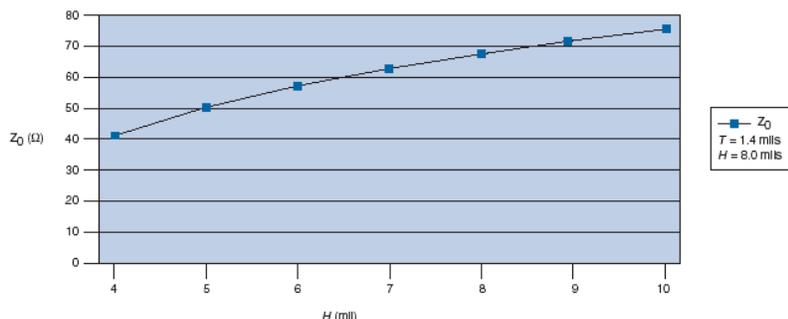


Figure 3. Microstrip Trace Impedance vs. Trace Height (H)

This figure shows the microstrip trace impedance vs. trace height (H), using the values in Equation 3, keeping trace width and trace thickness constant.

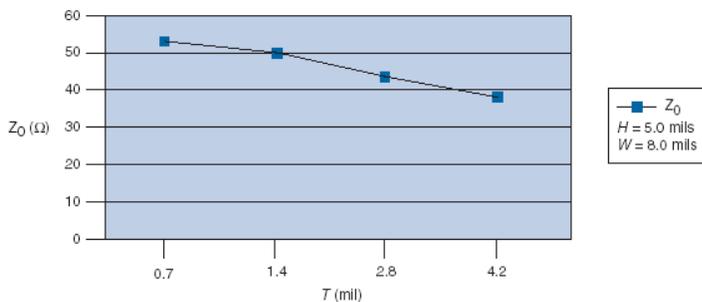


Figure 4. Impedance vs. Trace Thickness (T)

From the previous figures, we found the impedance is inversely proportional to trace width and directly proportional to trace height above the ground plane. This figure shows impedance vs. trace thickness (T) using the values in Equation 3, keeping trace width and dielectric height constant.

### 2.1.2 Stripline Impedance

A circuit trace routed on an inside layer of the PCB with two low-voltage reference planes (such as, power and / or GND) constitutes a stripline layout. You can use Equation 5 to calculate the impedance of a microstrip trace layout.

Eqn. 5

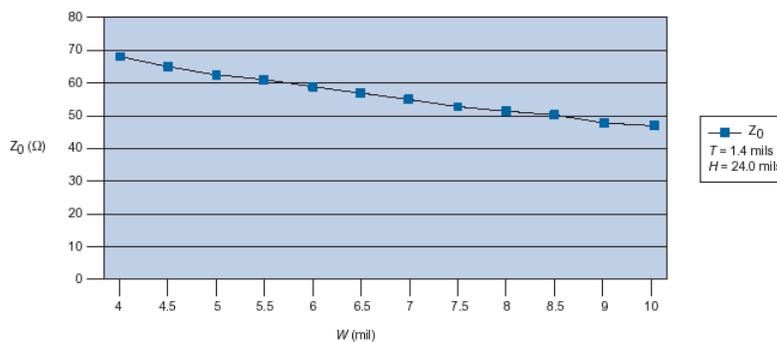
Using the typical values of W = 9 mil, H = 24 mil, T = 1.4 mil,  $\epsilon_r$  and (FR-4) = 4.1 with Equation 5 and solving for microstrip impedance (Z) yields the result of Equation 6 and Figure 5. The measurement unit in mils.

$$Z_o = \frac{60}{\sqrt{\epsilon_r}} \cdot \log\left(\frac{4 \times H}{0.67\pi(T + 0.8W)}\right) \cdot \Omega$$

In [Figure 5](#), [Figure 6](#), and [Figure 7](#), we found the impedance is inversely proportional to trace width and directly proportional to trace height above the ground plane. However, the rate of change with trace height above GND is much slower in a stripline layout compared with a microstrip layout. A stripline layout has a signal sandwiched by FR-4 material, whereas a microstrip layout has one conductor open to air. This exposure causes a higher, effective dielectric constant stripline layout compared to microstrip layouts. Thus, to achieve the same impedance, the dielectric span must be greater in stripline layouts compared with microstrip layouts. Therefore, stripline layout PCBs with controlled impedance lines are thicker than microstrip layout PCB.

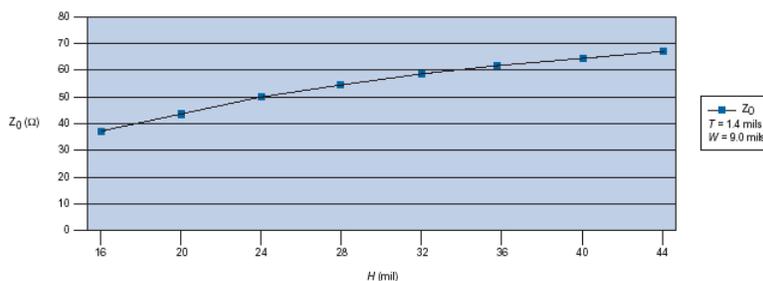
**Eqn. 6**

$$Z_o = \frac{60}{\sqrt{4.1}} \cdot \log\left(\frac{4 \times (24)}{0.67\pi(1.4) + 0.8(9)}\right) \approx 50\Omega$$



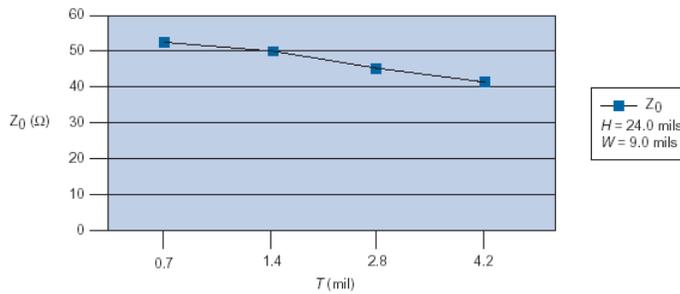
This figure shows the stripline trace impedance vs. trace width (W) using values in [Equation 5](#), keeping dielectric height and trace thickness constant.

**Figure 5. Stripline Trace Impedance vs. Trace Width (W)**



This figure shows the stripline trace impedance vs. trace height (H), using the values in [Equation 5](#), keeping trace width and trace thickness constant.

**Figure 6. Stripline Trace Impedance vs. Trace Height (H)**



This figure shows the stripline trace impedance vs. trace thickness (T) using the values in Equation 5, keeping trace width and dielectric height constant.

**Figure 7. Stripline Trace Impedance vs. Trace Thickness (T)**

Equation 7 and Equation 8 are used to calculate the relationship between propagation delay (T<sub>PD</sub>) or the time required for a signal to travel from one point to another. Transmission line propagation delay is a function of the dielectric constant of the material. Figure 8 shows the correlation between propagation delay and dielectric constant for microstrip and stripline traces.

**Microstrip Layout Propagation Delay**

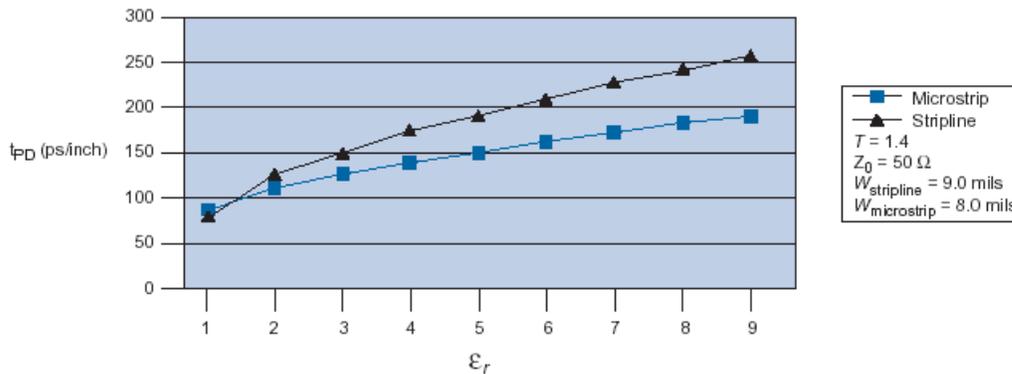
*Eqn. 7*

$$T_{PD} = 85 \cdot \sqrt{0.475\epsilon_r + 0.67} \cdot s$$

**Stripline Layout Propagation Delay**

*Eqn. 8*

$$T_{PD} = 85 \cdot \sqrt{\epsilon_r} \cdot s$$



**Figure 8. Propagation Delay vs. Dielectric Constant For Microstrip and Stripline Traces**

## 2.2 On-Board Noise Source

The following sections describe on-board noise sources and how to reduce their impact.

### 2.2.1 Crosstalk

Crosstalk is the unwanted coupling of signals between parallel traces. Proper routing and layer stack-up through microstrip and stripline layouts can minimize crosstalk.

To reduce crosstalk in dual-stripline layouts, which have two signal layers next to each other, route all traces perpendicular, increase the distance between the two signal layers, and minimize the distance between the signal layer and adjacent plane.

Use the following steps to reduce crosstalk in either microstrip or stripline layouts:

- Widen spacing between signal lines as much as routing restrictions will allow. Try not to bring traces closer than three times the dielectric height.
- Design the transmission line so that the conductor is as close to the ground plane as possible. This technique will couple the transmission line tightly to the ground plane and help decouple it from adjacent signals.
- Use differential routing techniques where possible, especially for critical nets (i.e., match the lengths as well as the gyrations that each trace goes through).
- If there is significant coupling, route single-ended signals on different layers orthogonal to each other.

Minimize parallel run lengths between single-ended signals. Route with short parallel sections and minimize long, coupled sections between nets.

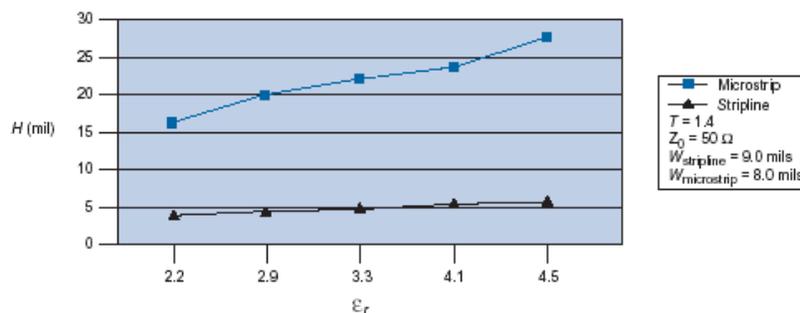
Crosstalk also increases when two or more single-ended traces run parallel and are not spaced far enough apart. The distance between the centers of two adjacent traces should be at least four times the trace width. To improve design performance, lower the distance between the trace and the ground plane to under 10 mils without changing the separation between two traces.

## 2.2.2 Signal Integrity

For a single-ended trace, like clock transmission line, it could be improved using the following guidelines:

- Keep clock traces as straight as possible. Use arc-shaped traces instead of right-angle bends.
- Do not use multiple signal layers for clock signals.
- Do not use via in clock transmission lines. Via can cause impedance change and reflection.
- Place a ground plane next to the outer layer to minimize noise. If you use an inner layer to route the clock trace, sandwich the layer between reference planes.
- Terminate clock signals to minimize reflection.
- Use point-to-point clock traces as much as possible.

For differential trace, [Figure 9](#) shows proper routing techniques are important for high-speed design. [Figure 10](#) is an example of separating traces for crosstalk.



**Figure 9. Height vs. Dielectric Constant Using Equation 3 and 5, Keeping Impedance, Width, and Thickness Constant**

- Make sure  $D > 2S$  to minimize the crosstalk between the two differential pairs.

### Design Consideration

- To minimize reflection noise, place the differential traces  $S = 3H$  as they leave the device.
- Keep the distance between the differential traces ( $S$ ) constant over the entire trace length.
- Keep the length of the two differential traces the same to minimize the skew and phase difference.
- Avoid using multiple via, because they can cause impedance mismatch and inductance.

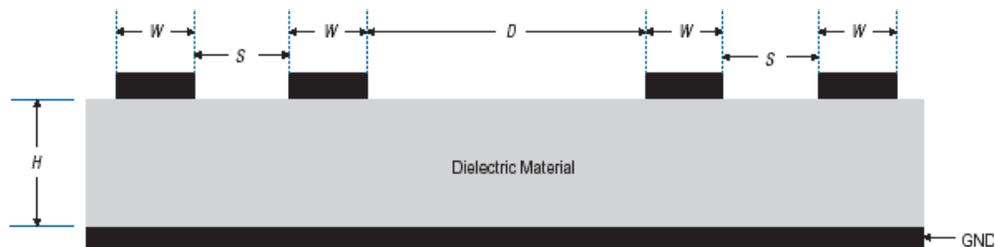


Figure 10. Example of Separating Traces for Crosstalk

## 2.2.3 Power Noise Filtering

To decrease the low-frequency (below 1 kHz) noise caused by the power supply, filter the noise on power lines at the point where the power connects to the PCB and to each device. Place a 100  $\mu\text{F}$  electrolytic capacitor where the power supply lines enter the PCB. If you use a voltage regulator, place the capacitor immediately after the pin that provides the VCC signal to the device(s). (Capacitors not only filter low-frequency noise from the power supply, but also supply extra current when many outputs switch simultaneously in a circuit.)

To filter power supply noise, use a non-resonant, surface-mount ferrite bead large enough to handle the current in series with the power supply. Place a 10 to 100  $\mu\text{F}$  bypass capacitor next to the ferrite bead. (If proper termination, layout, and filtering eliminate enough noise, you do not need to use a ferrite bead.) The ferrite bead acts as a short for high frequency noise coming from the VCC source. Any low frequency noise is filtered by a large 10  $\mu\text{F}$  capacitor after the ferrite bead. Usually, elements on the PCB add high-frequency noise to the power plane. To filter the high-frequency noise at the device, place decoupling capacitors as close as possible to each VCC and GND pair. Figure 11 is an example of a power noise filter.

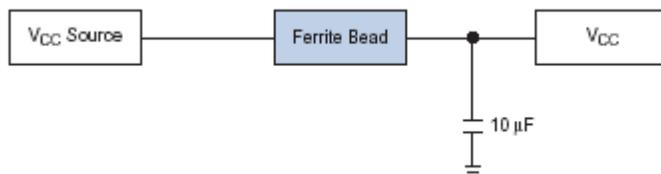
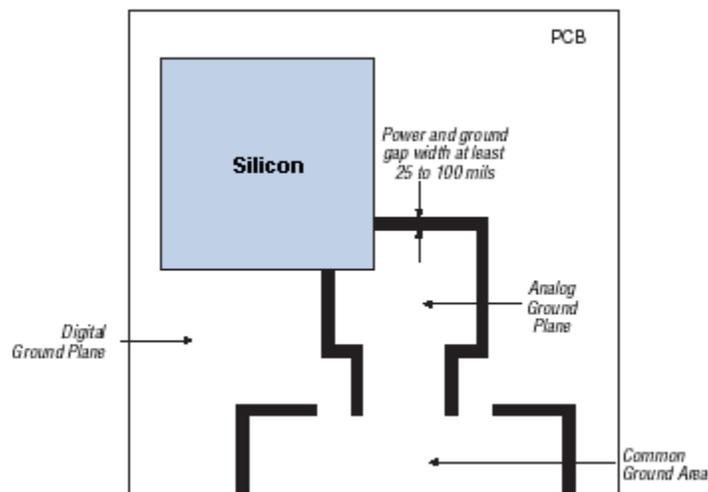


Figure 11. Power Noise Filtering Example

## 2.2.4 Power Distribution

A system can distribute power throughout the PCB with either power planes or a power bus network. You can use power planes on multi-layer PCBs that consist of two or more metal layers that carry VCC and GND to the devices. Because the power plane covers the full area of the PCB, its DC resistance is very low. The power plane maintains VCC and distributes it equally to all devices while providing very high current-sink capability, noise protection, and shielding for the logic signals on the PCB. It is recommended to use lower planes to distribute power. The power bus network which consists of two or more wide metal traces that carry VCC and GND to devices

is often used on two-layer PCBs and is less expensive than power planes. When designing with power bus networks, be sure to keep the trace widths as wide as possible. The main drawback to using power bus networks is significant DC resistance. It is recommended to separate analog and digital power planes. For fully digital systems that do not already have a separate analog power plane, it can be expensive to add new power planes. However, you can create partitioned islands (split planes). An example board layout with phase-locked loop (PLL) ground islands is shown on [Figure 12](#).



**Figure 12. Example Board Layout with Phase Locked Loop (PLL) Ground Islands**

If your system shares the same plane between analog and digital power supplies, there may be unwanted interaction between the two circuit types. The following suggestions will help to reduce noise:

- For equal power distribution, use separate power planes for the analog (PLL) power supply. Avoid using trace or multiple signal layers to route the PLL power supply.
- Use a ground plane next to the PLL power supply plane to reduce power-generated noise.
- Place analog and digital components only over their respective ground planes.
- Use ferrite beads to isolate the PLL power supply from digital power supply.

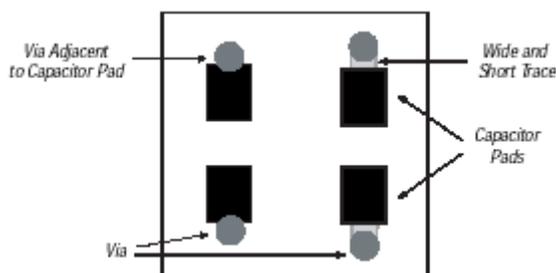
### 2.2.5 Ground Bounce

As digital devices become faster, their output switching times decrease. Faster switching times cause higher transient currents in outputs as they discharge load capacitances. These higher currents, which are generated when multiple outputs of a device switch simultaneously from a logic high to a logic low, can cause a board-level phenomenon known as Ground Bounce. Many factors contribute to ground bounce. Therefore, no standard test method predicts ground bounce magnitude for all possible PCB environments. Determine each condition and each device's relative contributions to ground bounce by testing the device under these conditions. Load capacitance, socket inductance, and the number of switching outputs are the predominant conditions that influence the magnitude of ground bounce in programmable logic devices.

It is recommended to follow some design methods to reduce ground bounce:

- Use wide, short traces between the via and capacitor pads, or place the via adjacent to the capacitor pad.

- Traces stretching from power pins to a power plane (or island, or a decoupling capacitor) must be as wide and as short as possible. This reduces series inductance, and therefore, reduces transient voltage drops from the power plane to the power pin. Thus, reducing the possibility of ground bounce.
- Connect each ground pin or via to the ground plane individually. A daisy chain connection to the ground pins shares the ground path, which increases the return current loop and thus inductance.



**Figure 13. Capacitor Pad Layout**

- Add the recommended decoupling capacitors for as many VCC/GND pairs as possible.
- Place the decoupling capacitors as close as possible to the power and ground pins of the device.
- Add external buffers at the output of a counter to minimize the loading on silicon device pins.
- Configure the unused I/O pin as an output pin and then drive the output low. This configuration acts as a virtual ground. Connect this low driving output pin to GNDINT and/or the boards ground plane.
- Configure the unused I/O pins as output, and drive high to prevent VCC sag.
- Turn on the slow slew rate logic option when speed is not critical.
- Limit load capacitance by buffering loads with an external device, such as the 74244 IC bus driver, or by reducing the number of devices that drive the bus.
- Eliminate sockets whenever possible.
- Reduce the number of outputs that can switch simultaneously and/or distribute them evenly throughout the device.
- Move switching outputs close to a package ground pin.
- Create a programmable ground next to switching pins.
- Eliminate pull-up resistors or use pull-down resistors.
- Use multi-layer PCBs that provide separate VCC and ground planes to utilize the intrinsic capacitance of GND-VCC plane.
- Add 10 to 30 ohm resistors in series to each of the switching outputs to limit the current flow into each of the outputs.
- Create synchronous designs that will not be affected by momentarily switching pins.
- Assign I/O pins to minimize local bunching of output pins.
- Place the power and ground pins next to each other. The total inductance will be reduced by mutual inductance, since current flows in opposite directions in power and ground pins.

- Use a bigger via size to connect the capacitor pad to the power and ground plane to minimize the inductance in decoupling capacitors.
- Use surface mount capacitors to minimize the lead inductance.
- Use low effective series resistance (ESR) capacitors. The ESR should be  $< 400$  m/ohm.
- Each GND pin/via should be connected to the ground plane individually.
- To add extra capacitance on the board, It is recommended to place a ground plane next to each power (VCC) plane. This placement gives zero lead inductance and no ESR. The dielectric thickness between the two planes should be  $\sim 5$  mils.

Analyzing Ground Bounce—Figure 14, shows a simple model for analyzing ground bounce. The external components driven by the device appear as capacitance loads to that device ( $C_1$  to  $C_n$ ). These capacitive loads store a charge determined by the following equation:

$$\text{Charge (Q)} = [\text{voltage (V) capacitance (C)}] \quad \text{Eqn. 9}$$

Thus, the charge increases as the voltage and/or load capacitance increase. A device's environment and ground path have intrinsic inductances (shown in the above diagram as  $L_1$ ,  $L_2$ , and  $L_3$ ).  $L_1$  is the inductance of the bond wire from the device's die to its package pin, and of the pin itself.  $L_2$  is the inductance of the connection mechanism between the device's ground pin and the PCB. This inductance is greatest when the device is connected to the PCB through a socket.  $L_3$  is the inductance of the PCB trace between the device and the PCB location where the power supply's reference ground is connected.

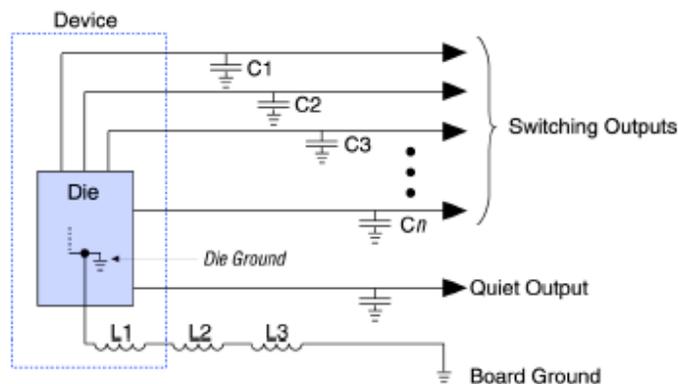


Figure 14. Simple Model for Analyzing Ground Bounce

Ground bounce occurs when multiple outputs switch from high to low. The transition causes the charge stored in the load capacitances to flow into the device. The sudden rush of current ( $di/dt$ ) exits the device through the inductances ( $L$ ) to board ground, generating a voltage ( $V$ ) determined by the equation  $V = L (di/dt)$ . This voltage difference between board ground and device ground causes the relative ground level for low or quiet outputs to temporarily rise or bounce. Although the rush of current is brief, the magnitude of the bounce can be large enough to trigger other devices on the PCB. In synchronous designs, ground bounce is less often a problem because synchronous outputs have enough time to settle before the next clock edge. Also, synchronous circuits are not as likely to be falsely triggered by a voltage spike on a quiet output. Capacitive loading on the switching outputs and quiet outputs affect ground bounce differently.

Minimizing Lead Inductance—Socket usage and PCB trace length are two elements of  $L_2$ , as shown in the previous diagram. Sockets can cause ground bounce voltage to increase by as much

as 100%. Eliminating sockets can often reduce the ground bounce on the PCB. The length of the PCB trace has a much smaller effect on ground bounce as compared to sockets. For PCBs with a ground plane, the voltage drop across the inductance ( $L_3$ ) of the PCB trace between the device and the PCB location where other devices in the system reference ground is negligible, because  $L_3$  is significantly less than  $L_2$ . The inductance in a 3-inch trace increases ground bounce for a quiet output by approximately 100 mV. Therefore, keep trace length to a minimum. As traces become longer, transmission line effects may cause other noise problem.

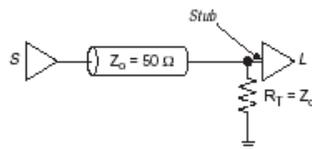
Using multi-layer PCBs that provide separate VCC and ground planes can also reduce the ground bounce caused by PCB trace inductance. Wire wrapping the VCC and ground supplies usually increases the amount of ground bounce. To reduce unwanted inductance, use low-inductance bypass capacitors between the VCC supply pins and the board ground plane, as close to the package supply pins as possible. The silicon requires low ESR decoupling surface mount capacitors of 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$  to be used in parallel to reduce ground bounce. Adding a 0.001  $\mu\text{F}$  capacitor in parallel to these capacitors filters high frequency noise (>100 MHz).

## 2.2.6 Termination Schemes

Mismatched impedance causes signals to reflect back and forth along the lines, which causes ringing at the load receiver. The ringing reduces the dynamic range of the receiver and can cause false triggering. To eliminate reflections, the impedance of the source ( $Z_S$ ) must equal the impedance of the trace ( $Z_0$ ), as well as the impedance of the load ( $Z_L$ ). This section discusses the following signal termination schemes:

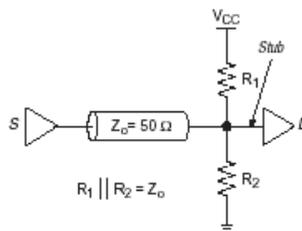
- Simple parallel termination
- Thevenin parallel termination
- Active parallel termination
- Series-RC parallel termination
- Series termination

**Simple Parallel Termination**—In a simple parallel termination scheme, the terminating resistor ( $R_T$ ) is equal to the line impedance. Place the termination resistor as close to the load as possible to be efficient.

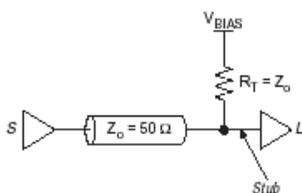
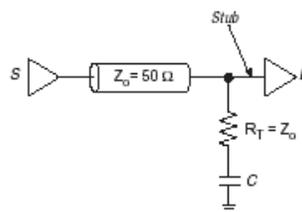
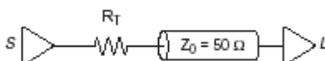


**Figure 15. Simple Parallel Termination**

**Thevenin Parallel Termination**—An alternative parallel termination scheme uses a Thevenin voltage divider. The terminating resistor is split between  $R_1$  and  $R_2$ , which equals the line impedance when combined. Although this scheme reduces the current drawn from the source device, it adds current drawn from the power supply because the resistors are tied between VCC and GND.


**Figure 16. Thevenin Parallel Termination**

Active Parallel Termination—An active parallel termination scheme, the terminating resistor ( $R_T = Z_0$ ) is tied to a bias voltage ( $V_{BIAS}$ ). In this scheme, the voltage is selected so that the output drivers can draw current from the high and low-level signals. However, this scheme requires a separate voltage source that can sink and source currents to match the output transfer rates.


**Figure 17. Active Parallel Termination**

**Figure 18. Series-RC Parallel Termination**

**Figure 19. Series Termination**

Series-RC Parallel Termination—A series-RC parallel termination scheme uses a resistor and capacitor (i.e., series-RC) network as the terminating impedance. The terminating resistor ( $R_T$ ) is equal to  $Z_0$ . The capacitor must be large enough to filter the constant flow of DC current. However, if the capacitor is too large, it will delay the signal beyond the design threshold. Capacitors smaller than 100 pF diminish the effectiveness of termination. The capacitor blocks low-frequency signals while passing high-frequency signals. Therefore, the DC loading effect of  $R_T$  does not have an impact on the driver, as there is no DC path to ground. The series-RC termination scheme requires balanced DC signaling (i.e., the signals spend half the time on and half the time off). AC termination is typically used if there is more than one load.

Series Termination—In a series termination scheme, the resistor matches the impedance at the signal source instead of matching the impedance at each load. The sum of  $R_T$  and the impedance of the output driver should be equal to the  $Z_0$ . Because Silicon output impedance is low, you should add a series resistor to match the signal source to the line impedance. The advantage of series termination is that it consumes

little power. However, the disadvantage is that the rise time degrades due to the increased RC time constant. Therefore, for high-speed designs, you should perform the pre-layout signal integrity simulation with silicon input/output buffer information specification (IBIS) models before using the series termination scheme.

### 3 MC9328MX1 Case Study

The critical high speed signals are associated with the SDRAM and SyncFlash memory interface. The clock signal, SDCLK, of the SDRAM and SyncFlash interface is targeted at 96 MHz. Two cases have been analyzed, the MC9328MX1 ADS v1.1 and a PDA form factor design, referred to as Demo v0.1.

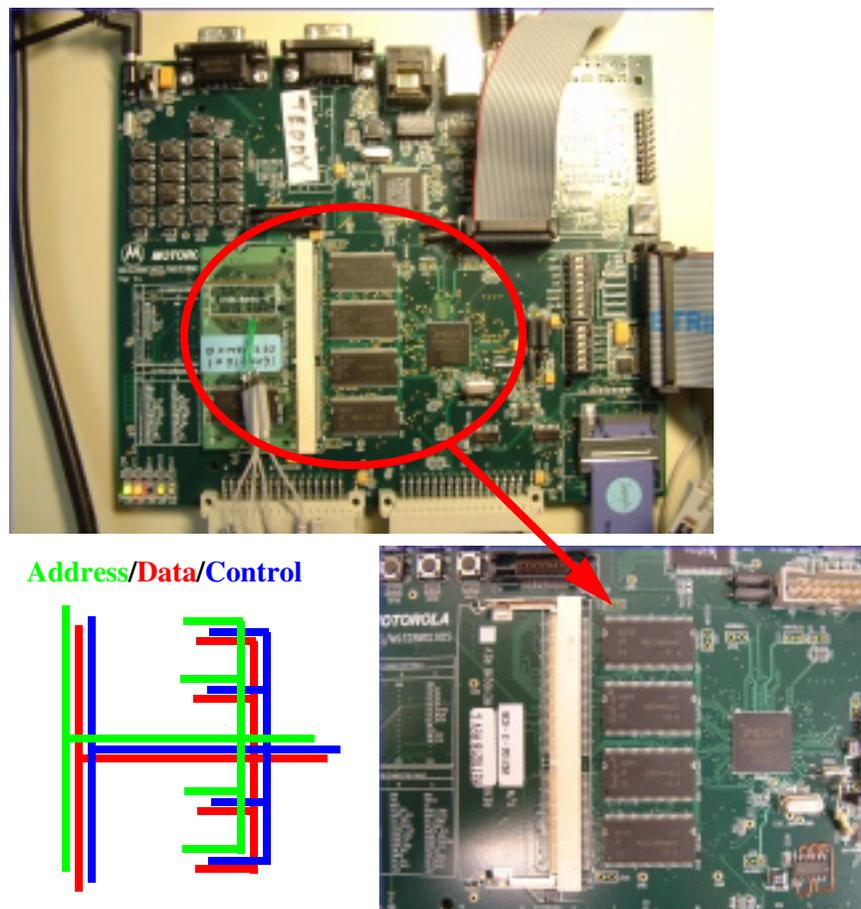
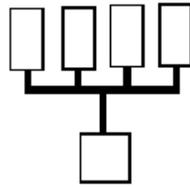


Figure 20. MC9328MX1 ADS v1.1 Development Board and Layout Scheme

#### 3.1 MC9328MX1 EVB v3.0 (ADS v1.1)

The Application Development System version 1.1 (ADS v1.1) was derived from the Evaluation Board version 3.0 (EVB v3.0), where a portion of the memory bus connections are the same. The development board is designed to exercise most features of the i.MX and has an extra socket for memory bus extension, known as the SODIMM connector. Also in this PCB design, we minimize the use of vias by placing the SyncFlash memory and SDRAM memory chips on the same side of PCB. This layout method results in

lower trace resistance, inductance and capacitance. Refer to [Figure 20](#) for an illustration of the ADS v1.1 system under evaluation.



**Figure 21. Recommend Layout of Memory Devices**

Following is the requirement list we applied to this development board:

- Place the 32 kHz and 16 MHz crystals close to the core and use short traces to connect the crystal to the XTAL and EXTAL pins.
- Prevent routing any high speed trace across or close to the 32 kHz crystal, 16 MHz crystal, XTAL pins and EXTAL pins. If possible, it is recommended to place a “route keep out” area around the crystal circuit.
- The total metal delay of each high speed trace should be smaller than 940 ps. This figure is based on the worst case 32-bit system with two 4M × 16-bit SyncFlash devices (MT28S4M16LC-10) and two 16M × 16-bit SDRAMs (MT48LC16M16A2-75). This figure can be larger if fewer memory devices are in the system or if SyncFlashes are not used. The setup time requirement of SyncFlash (MT28S4M16LC-10) is at least 3 ns while the setup time requirement of SDRAM (MT48LC16M16A2-75) is at least 1.5 ns. A longer trace will increase the rise time and the fall time of the signals therefore the setup time of signals generated by the i.MX will decrease with increased trace length.
- Place the memory devices with the larger setup time closer to the i.MX and connect them with shorter traces. For example, SyncFlash has a 3 ns setup time and SDRAM has a 2 ns setup time. Therefore the SyncFlash should be placed closer to the i.MX.
- Connect the signal which has higher priority with shorter trace. The priority of the signals are as follows:

Priority	Highest	10	9	8	7	6	5	4	3	2	1	Lowest
Signals	SDCLK	Addr	CAS	RAS	SDWE	CS3	CS2	Data	DQM	SDCKE1	SDCKD0	RP

**Figure 22. Priority Signals**

- Use as few vias as possible to avoid adding extra capacitance loading to the trace.
- Use a Tee topology for the PCB layout of the trace to balance the delay between the i.MX to different memory devices. [Figure 21](#) provides an illustration of this.
- It is recommended to add one 0.01 μF decoupling capacitor and one 0.1 μF decoupling capacitor for each memory device’s power supply to ground.

With the ADS v1.1 PCB, we have measured the worst case trace from the SDCLK relative to Address, Data or Controls signals. Also, the board vendor was able to perform a simulation of the ADS v1.1 memory signals routing and provide the trace data for these signals. From their simulation data and concurrently from capturing the waveforms from this signal it was found that Address signal A2 is the worst signal on

the board relative to the SDCLK, providing the worst case set up time measurement. This simulation data, as well as the captured waveforms can be found in Figure 23. Also, Figure 24 provides a logical illustration of memory signals routing.

NET = A2 (The whole trace incl. the route to Socket)

**COUNTS**

segments	34
IC drivers	0
IC receivers	7
resistors	0
capacitors	0

**INTERCONNECT STATISTICS**

total metal delay	707.073 ps
minimum metal Z0	41.7 ohms
maximum metal Z0	59.2 ohms
total metal capacitance	15.4 pF
total metal inductance	33.3 nH
total metal resistance	297.7 milliohms
total metal length	010.405 cm
average metal Z0	46.5 ohms

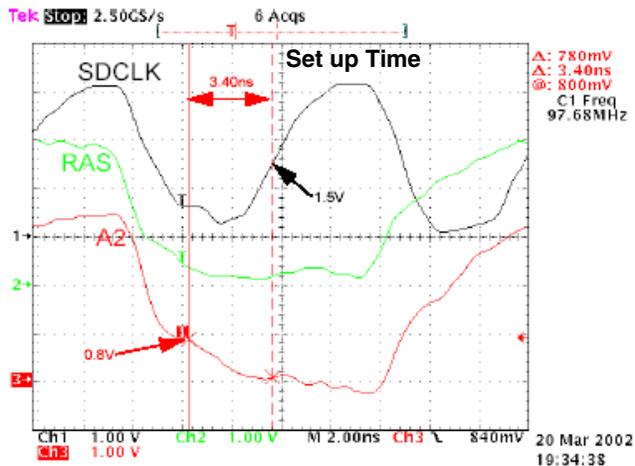
NET = SDCLK (The whole trace incl. the route to Socket)

**COUNTS**

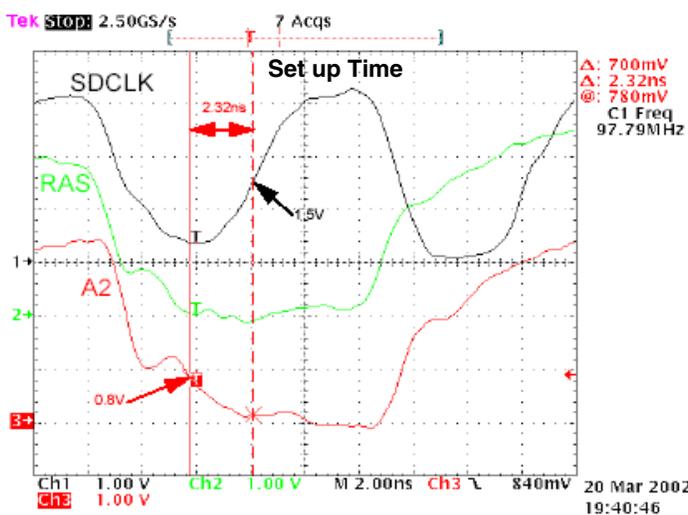
segments	32
IC drivers	0
IC receivers	7
resistors	0
capacitors	0

**INTERCONNECT STATISTICS**

total metal delay	904.342 ps
minimum metal Z0	28.8 ohms
maximum metal Z0	45.1 ohms
total metal capacitance	23.5 pF
total metal inductance	34.9 nH
total metal resistance	212.1 milliohms
total metal length	014.292 cm
average metal Z0	38.5 ohms



SyncFlash



SDRAM

Figure 23. PCB Vendor’s Simulated Trace Data and Waveforms Captured from the ADS v1.1

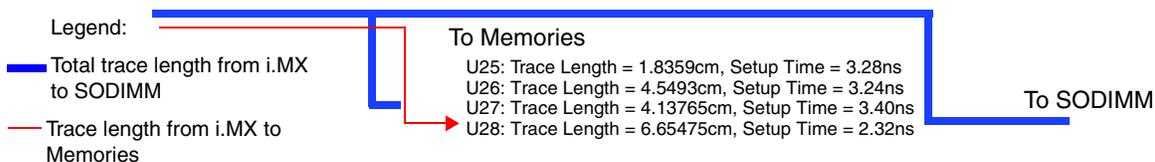


Figure 24. Trace Layout Illustration for the ADS v1.1 Memory System

The address line A2 is connected to two SDRAMs and two SyncFlashes. The worst waveform was captured on the memory device pin A2 (Figure 23). This is referenced to the SDCLK signal at the SDCLK pin of same device.

Considering the setup time requirement, the connection length between the memory and the i.MX is suggested to be within 4.5 cm (indicated by the red line in [Figure 24](#)) and it is recommended the total metal delay should be smaller than 940 ps, trace inductance within 40 nH and trace capacitance no larger than 20 pF. With ADS v1.1, a standard memory test program is executed (refer to Section 5, “References,” on page 24). It shows smooth execution up to 96 MHz with a 3.0 V memory bus (0–70 degrees). In an experiment to test bus speed at 1.8 V, 1.8 V SDRAM was placed on a separate board connected to the SODIMM connector and it was found to operate stable up to 86 MHz. However, it should be noted that adding memories via the SODIMM connector increases both trace length and bus loading. Section 3.2, “MC9328MX1 Demo v0.1,” will address this issue with the design of a PDA form factor style board.

### 3.2 MC9328MX1 Demo v0.1

With the ADS v1.1, we found the memory access at 96 MHz unstable at 1.8 V. To achieve the system stability at 96 MHz with a 1.8 V bus, the memories should be placed on the same PCB as close as possible to the i.MX and not on a separate PCB connected via the SODIMM. This improves the setup time of the memory bus. A PDA form factor board using this guideline was created and in this trial, we observed the R, L, and C are greatly improved. [Figure 25](#) provides a picture of the form factor PCB and illustrates the memory configuration (two 16-bit SDRAMs and one 32-bit Disk On Chip (DOC)). While [Figure 26](#) lists the PCB layer description. [Figure 27](#) provides details of the memory devices capacitive loading, and [Figure 28](#) shows the PDA form factor design in its casing. [Figure 29](#) details the simulation data and the characteristics of the worst case signals from Address, Data and Control traces relative to the SDCLK trace, provided by the board vendor.



**Figure 25. MC9328MX1 Demo v0.1 PCB Illustrating the Memory Layout: 2 × 16-bit SDRAMs and 1 × 32-bit DOC**

Layer	8	7	6	5	4	3	2	1
Signals	Signal	Power	Signal	Signal	Signal	Signal	GND	Signal

**Figure 26. MC9328MX1 Demo v0.1 PCB Layer Description**

Cap. Loading	6pF	4pF	4pF	4pF	6.5pF	6.5pF	4.7pF	6.5pF
Signals	Data pin	Address pin	Control pin	Clock pin	Data pin	Address pin	Control pin	Clock pin
	SDRAM				Flash (DOC)			

**Figure 27. MC9328MX1 Demo v0.1 Device Capacitive Loading**



Figure 28. MC9328MX1 Demo v0.1 PDA Form Factor Design

<b>NET = SDCLK</b>	
<b>INTERCONNECT STATISTICS</b>	
total metal delay.....	290.740 ps
minimum metal Z0.....	52.5 ohms
maximum metal Z0.....	62.5 ohms
total metal capacitance.....	4.7 pF
(SDCLK.....)	4.7 pF)
total metal inductance.....	18.1 nH
(SDCLK.....)	18.1 nH)
total metal resistance.....	93.1 milliohms
(SDCLK.....)	93.1 milliohms)
total metal length.....	001.740 in
average metal Z0.....	62.1 ohms
<b>NET = A9</b>	
<b>INTERCONNECT STATISTICS</b>	
total metal delay.....	579.344 ps
minimum metal Z0.....	40.8 ohms
maximum metal Z0.....	55.4 ohms
total metal capacitance.....	13.0 pF
(A9.....)	13.0 pF)
total metal inductance.....	26.3 nH
(A9.....)	26.3 nH)
total metal resistance.....	354.5 milliohms
(A9.....)	354.5 milliohms)
total metal length.....	003.319 in (001.823 in for the SDRAM segment)
average metal Z0.....	45.0 ohms
<b>NET = D13</b>	
<b>INTERCONNECT STATISTICS</b>	
total metal delay .....	343.398 ps
minimum metal Z0 .....	40.8 ohms
maximum metal Z0 .....	55.4 ohms
total metal capacitance .....	6.9 pF
(D13 .....	6.9 pF)
total metal inductance .....	17.5 nH
(D13 .....	17.5 nH)
total metal resistance .....	209.4 milliohms
(D13 .....	209.4 milliohms)
total metal length .....	001.966 in
average metal Z0 .....	50.5 ohms
<b>NET = ~SDWE</b>	
<b>INTERCONNECT STATISTICS</b>	
total metal delay .....	301.177 ps
minimum metal Z0 .....	52.5 ohms
maximum metal Z0 .....	55.4 ohms
total metal capacitance .....	5.5 pF
(~SDWE .....	5.5 pF)
total metal inductance .....	16.5 nH
(~SDWE .....	16.5 nH)
total metal resistance .....	171.0 milliohms
(~SDWE .....	171.0 milliohms)
total metal length .....	001.703 in
average metal Z0 .....	54.8 ohms

**Figure 29. MC9328MX1 Demo v0.1 Simulation Data and Characteristics of the Worst Case Signals From the Clock, Address, Data and Control Traces**

Comparing the trace length and setup time, the connection between the memory and the i.MX should not be longer than 4 cm (< 65 ohm) and it is recommended the total metal delay should be smaller than 800 ps, trace inductance should be smaller than 28 nH and trace capacitance should under 15 pF.

The PCB design were:

- 8-layer (refer to [Figure 26](#))
- $\epsilon_r$  for FR-4 is 4.1

- Copper trace width = 6 mil (rings are not added in the inter-layer of the vias)
- Via size = 20 mil (10 mil drill hole SDRAM each)
- (The form factor has two x16 SDRAMs and one x32 Flash - DOC)

Based on the current layout and component capacitive loading, we have:

- For SDCLK < (route:5 pF + chip:[4+4+4.7]=12.7 pF) = 17.7 pF
- For Address < (route:15 pF + chip:[4+4+6.5]=14.5 pF) = 29.5 pF
- For Data < (route: 7 pF + chip:[6+6.5]=12.5 pF) = 19.5 pF
- For Control < (route: 5.5 pF + chip:[4+4+4.7]=12.7 pF) = 18.2 pF

MC9328MX1 Demo v0.1 (PDA Form Factor Design) successfully achieves 96 MHz at both 3.0 V and 1.8 V memory bus voltages, up to 80 degrees C. To qualify the system stability, standard “bit-walk” memory tests were conducted on both a standalone (lightly loaded) and Linux OS (heavy loaded) environment from selected samples in each of the process corners (refer to Section 5, “References,” for details). Section 5 also provides the details of the selected sample for this qualification test. Finally, please refer to Section 4, “Design Guidelines on PCB,” for a summary of recommended guidelines for designing a high speed low-power PCB using the i.MX.

## 4 Design Guidelines on PCB

The following recommendations are to design high-speed, low-power PCBs for i.MX silicon:

- Widen spacing between signal lines as much as routing restrictions will allow. Try not to bring traces closer than three times the dielectric height.
- Design the transmission line so that the conductor is as close to the ground plane as possible. This technique will couple the transmission line tightly to the ground plane and help decouple it from adjacent signals.
- Use differential routing techniques where possible, especially for critical nets (such as, match the lengths as well as the gyrations that each trace goes through).
- If there is significant coupling, route single-ended signals on different layers orthogonal to each other.
- Minimize parallel run lengths between single-ended signals. Route with short parallel sections and minimize long, coupled sections between nets.
- Keep clock traces as straight as possible. Use arc-shaped traces instead of right-angle bends.
- Do not use multiple signal layers for clock signals.
- Do not use via in clock transmission lines. Via can cause impedance change and reflection.
- Place a ground plane next to the outer layer to minimize noise. If you use an inner layer to route the clock trace, sandwich the layer between reference planes.
- Terminate clock signals to minimize reflection.
- Use point-to-point clock traces as much as possible.
- Configure unused I/O pins as output pins, and drive the output low to reduce ground bounce. This configuration will act as a virtual ground.
- Configure the unused I/O pins as output, and drive high to prevent VCC sag.

- Turn on the slow slew rate logic option when speed is not critical.
- Eliminate sockets whenever possible.
- Depending on the problem, move switching outputs close to either a package ground or VCC pin. Eliminate pull-up resistors, or use pull-down resistors.
- Use multi-layer PCBs that provide separate VCC and ground planes to utilize the intrinsic capacitance of GND-VCC plane.
- Create synchronous designs that are not affected by momentarily switching pins.
- Add the recommended de-coupling capacitors to VCC/GND pairs.
- Place the decoupling capacitors as close as possible to the power and ground pins of the device.
- Connect the capacitor pad to the power and ground plane with larger via to minimize the inductance in decoupling capacitors and allow for maximum current flow.
- Use wide, short traces between the via and capacitor pads, or place the via adjacent to the capacitor pad.
- Traces stretching from power pins to a power plane (or island, or a decoupling capacitor) should be as wide and as short as possible. This reduces series inductance, and therefore, reduces transient voltage drops from the power plane to the power pin. Thus, reducing the possibility of ground bounce.
- Use surface-mount low effective series resistance (ESR) capacitors to minimize the lead inductance. The capacitors should have an ESR value as small as possible.
- Connect each ground pin or via to the ground plane individually. A daisy chain connection to the ground pins shares the ground path, which increases the return current loop and thus inductance.
- For equal power distribution, use separate power planes for the analog (PLL) power supply. Avoid using trace or multiple signal layers to route the PLL power supply.
- Use a ground plane next to the PLL power supply plane to reduce power-generated noise.
- Place analog and digital components only over their respective ground planes.
- Use ferrite beads to isolate the PLL power supply from digital power supply.
- Add the recommended decoupling capacitors for as many VCC/GND pairs as possible.
- Place the decoupling capacitors as close as possible to the power and ground pins of the device.
- Add external buffers at the output of a counter to minimize the loading on silicon device pins.
- Configure the unused I/O pin as an output pin and then drive the output low. This configuration acts as a virtual ground. Connect this low driving output pin to GNDINT and/or the boards ground plane.
- Limit load capacitance by buffering loads with an external device, such as the 74244 IC bus driver, or by reducing the number of devices that drive the bus.
- Eliminate sockets whenever possible.
- Reduce the number of outputs that can switch simultaneously and/or distribute them evenly throughout the device.
- Move switching outputs close to a package ground pin.
- Create a programmable ground next to switching pins.
- Eliminate pull-up resistors or use pull-down resistors.

- Use multi-layer PCBs that provide separate VCC and ground planes.
- Add 10 to 30 ohm resistors in series to each of the switching outputs to limit the current flow into each of the outputs.
- Create synchronous designs that will not be affected by momentarily switching pins.
- Assign I/O pins to minimize local bunching of output pins.
- Place the power and ground pins next to each other. The total inductance will be reduced by mutual inductance, since current flows in opposite directions in power and ground pins.
- Use a bigger via size to connect the capacitor pad to the power and ground plane to minimize the inductance in decoupling capacitors.
- Use surface mount capacitors to minimize the lead inductance.
- Use low effective series resistance (ESR) capacitors. The ESR should be  $< 400$  ohm.
- Each GND pin/via should be connected to the ground plane individually.
- To add extra capacitance on the board, It is recommended to place a ground plane next to each power (VCC) plane. This placement gives zero lead inductance and no ESR. The dielectric thickness between the two planes should be  $\sim 5$  mils.
- Place suitable termination resistor to ensure impedance matching between the line impedance ( $R_O$ ) and the terminating resistor ( $R_T$ ) is equal to the line impedance.
- Recommendations for critical high speed routing, such as SDRAMC related signals for 3.0 V memory bus:
  - Trace length under 4.5 cm, less than 65 ohm, to maintain the metal delay within 940 ps.
  - Inductance value of that trace less than 40 nH.
  - Keep the trace capacitance within 20 pF.
  - Overall capacitive loading (including both trace and component) for all signals, Address, Data, Control, and SDCLK, should be no greater than 30 pF.
- Recommendations for critical high speed routing, such as SDRAMC related signals for 1.8 V memory bus:
  - Trace length under 4 cm, less than 55 ohm, to maintain the metal delay within 800 ps.
  - Inductance value of that trace less than 28 nH.
  - Keep the trace capacitance within 15 pF.
  - From the data captured from the PDA form factor design, the following total capacitive loading (including both trace and component) is recommended for the following signals:
    - Address, Data, and Control signals: The Address bus displayed the highest total capacitive loading of 29.5 pF, and this same maximum can be applied to similar signals such as the Data and Control signals (like RAS, CAS, etc.). Thus we recommend a total capacitive loading of less than 30 pF for these signals.
    - SDCLK signal: Due to the importance of this signal for latching information, and the fact that all the other signals are dependent upon the integrity of this signal, it is highly recommend a total capacitive loading of this signal to be less than 18 pF.

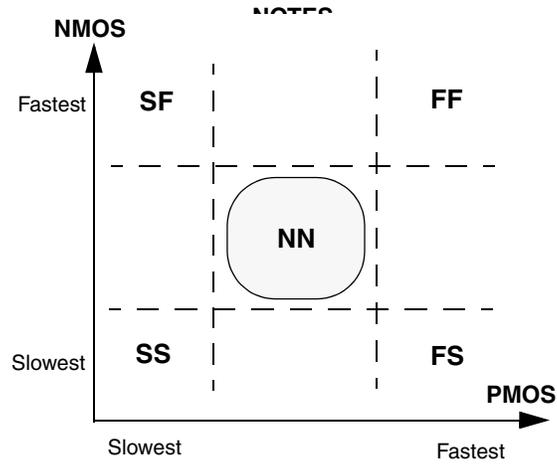
## 5 References

The following **books** were used as reference in writing this application:

1. *High-Speed Digital Design*, H.W. Johnson, and M. Graham, (Prentice Hall, 1993)
2. *High-Speed Digital System Design*, S. H. Hall, G. W. Hall, and J. A. McCall (John Wiley & Sons, Inc. 2000)
3. *High-Speed PCB Design Myths, ASIC & EDA*, Kella Knack (Los Altos: James C. Uhl, July 1993)

The following **tests** were used in writing this application:

1. Bit-walk memory test:
  - a) Clear the entire usable memory to zeros. In Linux, the user region of SDRAM is referred to as usable memory
  - b) Set bit[0] of the first word of the memory via a write operation
  - c) Read the entire usable memory to confirm only the previous set bit is ONE
  - d) Set LED via the GPIO to indicate failure if any bit was read incorrectly
  - e) Shift to bit[1] and repeat (b) through (d)
  - f) Continuing shifting up to bit[31] and for each shift repeat (b) through (d)
  - g) Continue to next word in the memory, and repeat (b) to (f), till end of the usable memory
  - h) Compile and execute on both standalone (limited for 10 Kilobyte) and Linux environment (limited for 4 Mbyte) under the room temperature and 80 degrees Celsius
2. Samples used for the qualification test:
  - a) Divided the process into 5 corners, see [Figure 30](#)
  - b) FF stands for PMOS fast process type, where  $V_T = -0.3930$  V; NMOS fast process type, where  $V_T = 0.3915$  V
  - c) FS stands for PMOS fast process type, where  $V_T = -0.3930$  V; NMOS slow process type, where  $V_T = 0.4284$  V
  - d) SF stands for PMOS slow process type, where  $V_T = -0.4284$ v; NMOS fast process type, where  $V_T = 0.3915$  V
  - e) NN stands for PMOS nominal process type, where  $V_T = -0.4172$ v; NMOS nominal process type, where  $V_T = 0.4172$  V
  - f) SS stands for PMOS slow process type, where  $V_T = -0.4284$  V; NMOS slow process type, where  $V_T = 0.4284$  V
  - g) Select 3 samples from each FF, FS, SF and NN, and 6 samples from SS
  - h) Put those selected samples on the MC9328MX1 Demo Board v0.1 and perform the Bit-walk memory test as mentioned above



**Figure 30. Process Corner Illustration**

## 6 Revision History

Table 2 shows the revision history of this document.

**Table 2. Revision History**

Revision Number	Comments
0	<ul style="list-style-type: none"> <li>Initial version</li> </ul>
1	<ul style="list-style-type: none"> <li>Applied Freescale Template</li> <li>Updated document includes i.MXS device</li> </ul>
2	<ul style="list-style-type: none"> <li>No content changes. Format only.</li> </ul>

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